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LIFO TYPE DATA STORAGE DEVICE INCORPORATING TWO RANDOM ACCESS MEMORIES

PRIORITY CLAIM

The present application claims priority from French Application for Patent No. 02 12663, filed October 11, 2002, the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[1] The present invention relates to a LIFO ("Last In, First Out") storage device, otherwise known as a reverse stack.

Description of Related Art

[2] A LIFO type storage device is characterized by a depth P, P being an integer which may be of the form 2^N, N being an integer. The function of the device is to store a succession of data produced by a data source in a determined chronological order, and to retrieve these data in successive sequences of P data, the chronological order of data retrieval within each sequence being the reverse of the chronological order of data production by the source. Storage by the device of data produced by the source continues simultaneously with data retrieval, in a timed manner according to a series of successive further defined time intervals. Thus, under the nominal operating conditions of the storage device, recording a datum and retrieving another datum takes place at each time interval.

[3] In a manner known to a person skilled in the art, a LIFO type storage device of depth P may consist of two identical single port random access memories (SP-RAM), each with P addresses, to which the sequences of P data are directed. In this type of device, the data from the same sequence may be directed to the same memory, alternating between the two RAM memories for two successive sequences of data. Thus, at each timing interval of the operation

of the storage device, a datum from a sequence being produced by the data source is written to one of the two SP-RAMs, while another datum from the immediately previous data sequence is simultaneously read in the other SP-RAM. To achieve reverse stack operation, each SP-RAM is read in the address order of this SP-RAM in the reverse order of the same addresses in which the data have been previously written to this SP-RAM.

[4] This type of storage device accordingly requires two SP-RAMs, each having at least as many addresses as depth P of the device. This large storage capacity entails a large cost, due in particular to the surface area of semiconductor substrate necessary for producing the corresponding memory modules.

[5] The storage capacity necessary for a LIFO type storage device of depth P can be reduced to a single RAM memory with P addresses, by using a DP-RAM (or Dual Port-RAM) type memory. At each timing interval of the storage device's operation, a datum from a sequence being produced by the data source can then be written to this DP-RAM, whilst another datum is simultaneously read in this DP-RAM from the immediately previous data sequence. This reading and writing take place at two successive addresses in an

address scanning of the DP-RAM. To achieve reverse stack operation, the data from the same sequence are written then read in the DP-RAM by scanning the addresses of the DP-RAM in reverse orders between reading and writing the data of this sequence. Under these circumstances, a single memory module with P addresses is sufficient.

[6] One drawback of this latter embodiment of LIFO type storage devices lies in the use of DP-RAM memory modules. This is because DP-RAM memory modules are more expensive and bulkier than SP-RAM memory modules for the same storage capacity. They are therefore especially limiting for the production of small, cheap circuits.

SUMMARY OF THE INVENTION

[7] The present invention proposes a LIFO type storage device of depth $P=2^N$, N being an integer, comprising two RAM memories each capable of having upwards of P/2 data entry addresses.

[8] A storage device according to the invention comprises:

two random access memories each having at least 2^{N-1} locations for storing data at respective addresses, N being an integer greater than 1, a data input connected to a data source, a command input, an address input and an output;

multiplexing means having first and second data inputs respectively connected to the data outputs of the two memories, a third data input connected to the data source and an output reproducing data present at one of said first, second and third data inputs, selected by switching signals;

a controller for issuing electrical signals, within successive time intervals, at outputs of the controller including two access command outputs respectively connected to the command inputs of the two memories, two address outputs respectively connected to the address inputs of the two memories and at least one switching command output for issuing said switching signals; and

means for sampling the multiplexing means output at the beginning of each time interval and producing device output data.

[9] The controller is set up in the invention's storage device to issue in the course of two consecutive sequences of 2^N time intervals:

on each of the two access command outputs, and for at least time intervals distinct from the boundaries of the two sequences, alternate read and write access commands, a write access command being issued on one of said access

command outputs while a read access command is issued on the other access command output and vice versa;

on each of the two address outputs, increasing addresses during one of the two sequences and decreasing addresses during the other sequence, such that, for at least time intervals distinct from the boundaries of the two sequences, the address input of each memory receives the same address in the course of two consecutive time intervals of each sequence during which the command input of said memory receives a read access command and then a write access command; and

on each switching command output, switching signals set so that in the course of each sequence, the sampling means produce data originating from the source in a reverse chronological order from the chronological order of arrival of said data from the source.

[10] A first advantage of a storage device according to the invention lies in its especially low energy consumption. This low consumption results in particular from its possible operation with a total of just 2^N memory locations, i.e. as many as the depth of the corresponding reverse stack, as defined earlier.

[11] A second advantage of a storage device according to the invention lies in its possible operation with SP-RAM type memories. This results in a significant saving in semiconductor substrate surface area, and consequently an especially low cost for the device.

[12] A storage device according to the invention can be used for various types of data. In particular, the data can be successions of bits such as bytes, programs or collections of information elements having to be produced in a reverse chronological order to that of arrival of these same data from a source appropriate to each type of data. So both of the memories of the device must have locations of a size appropriate to the type of data stored.

[13] In a preferred embodiment of the invention, the switching signals are issued in such a way that the output of the multiplexing means reproduces data present at said third data input, during at least one time interval at a boundary of each sequence. In this embodiment and during the time intervals concerned, the data issued by the source are reproduced at the output of the multiplexing means with a delay due to the multiplexing means only. The delay introduced by the storage device between the sequences of data produced at the output of the multiplexing means and

the sequences of the same data issued by the source is then minimal, while being compatible with the operation of the reverse stack.

[14] Storage devices according to the invention can be produced with different types of memories, including, in particular, deferred or immediate read SP-RAM memories. For deferred read SP-RAM memories, the data read are produced at the memory output during the time interval immediately following the time interval during which the command input of said memory receives a read access command and the address input of said memory receives an address. This first type of memory enables especially fast operation of the storage device. By contrast, data read in an immediate read SP-RAM memory are produced at the memory output during the same time interval during which the command input receives a read access command and the address input receives an address. This second type of memory can be adapted for storage devices incorporated into circuits further including memory modules of this type. It is, in fact, sometimes advantageous to use a single type of memory within the same circuit.

[15] The invention also relates to a method of data storage and retrieval using a storage device as previously disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[16] A more complete understanding of the method and apparatus of the present invention may be acquired by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[17] FIGURE 1 represents the architecture of a storage device according to the present invention;

[18] FIGURE 2 is a functional diagram of a controller adapted for a storage device according to FIGURE 1 using deferred read SP-RAM type memories; and

[19] FIGURE 3 is a functional diagram of a controller adapted for a storage device according to FIGURE 1 using immediate read SP-RAM type memories.

DETAILED DESCRIPTION OF THE DRAWINGS

[20] The circuit architecture of FIGURE 1 is common to both embodiments subsequently disclosed. The first embodiment uses two deferred read SP-RAM type memory modules, and the

second embodiment uses two immediate read SP-RAM type memory modules.

[21] According to FIGURE 1, the storage device possesses a data input E connected to a data source referenced 1000. This data input E is connected via respective data buses to the data input 18 of a first memory 10 of one of the types mentioned above, to the data input 19 of a second memory 20 of the same type, and to a first data input 41 of a multiplexer 40, marked MUX2 in FIGURE 1. The two memories are marked RAM1 and RAM2 in FIGURE 1.

[22] The outputs of the two memories 10, 20 are connected respectively via data buses to a first input 31 and to a second input 32 of a multiplexer 30, marked MUX1 in FIGURE 1. The data output of the multiplexer 30 (MUX1) is connected to a second data input 42 of the multiplexer 40 (MUX2).

[23] The output of the multiplexer 40 (MUX2) is connected to the input 51 of a flip-flop D referenced 50 in FIGURE 1, whose output 52 constitutes the data output S of the data storage device.

[24] According to a form of operation explained later on, the data issued by the source 1000 are distributed between a first group of data, marked DATA1 in FIGURE 1, which pass

through memory 10, a second group of data, marked DATA2, which pass through memory 20, and data transmitted directly between the input E of the device and the multiplexer 40 (MUX2).

[25] A clock, not shown, connected to the controller 1, to both multiplexers 30, 40 and to the flip-flop D 50 times the overall operation of the device according to a defined series of time intervals. The timing of the operation may also possibly be defined by interrogation and trigger signals transmitted to certain components of the storage device.

[26] A controller 1 responsible for controlling the storage device has the following outputs:

first and second access command outputs 12 and 13 connected to respective command inputs of memory 10 (RAM1) and memory 20 (RAM2). Each of the outputs 12, 13 transmits a binary access command R/W1 or R/W2 respectively, during each time interval. By way of example, a value 0 commands a write access in the memory 10, 20 concerned, and a value 1 commands a read access;

first and second address outputs 14 and 15 connected to respective address inputs of the memories 10 and 20 via respective address buses. The addresses ADDR1 and ADDR2 of

the memories 10 and 20 thus transmitted are coded by the controller 1 over N-1 bits, between 0 and $2^{N-1}-1$;

first and second switching command outputs 16 and 17 connected to the respective switching command inputs of the multiplexers 30 and 40. By way of example, the switching signals SW1 and SW2 produced respectively at the outputs 16 and 17 each have, for each time interval, a binary value of 0, when the output of the multiplexer 30/40 concerned is intended to reproduce the datum received at said first input 31/41 of this multiplexer, or a binary value of 1 when the output of this multiplexer 30/40 is intended to reproduce the datum received at said second input 32/42 of this multiplexer.

[27] Furthermore, each multiplexer 30/40 instantaneously reproduces at its output the data received at its first input 31/41 or at its second input 32/42 according to the switching signal SW1/SW2 transmitted at its switching command input. Thus, for each time interval, the output of each multiplexer 30, 40 reproduces the data received during this same time interval at one of its two inputs.

[28] The invention is now disclosed in detail according to a first embodiment using two deferred read SP-RAM type memory modules.

[29] Inside the controller 1 corresponding to FIGURE 2, a cyclic counter 100 produces a count number for the time interval in progress. This count number, over N+1 bits, i.e. between 0 and 2^{N+1}-1 bits, reverts to 0 when the value 2^{N+1} is reached. The counter 100 is synchronized with the operation timing system of the overall device via a link not shown.

[30] A first circuit branch within the controller 1, connected to the output of the counter 100, generates the access address ADDR1 to the memory 10 (RAM1) for each time interval. In this first branch, a first partial count number for the time interval in progress, over N-1 bits, is obtained by removing the most significant bit (MSB) and the least significant bit (LSB) from the count number issued by the counter 100. The removal of the end bits of the count number is done by the separator 101.

[31] The first partial count number is then sent directly to a first input of a multiplexer 105 inside the controller 1. A digital operator 103, operating over N-1 bits, subtracts the first partial count number from the number 2^{N-1}-2 and sends the result to a second input of the multiplexer 105.

[32] The output of the multiplexer 105 is connected to the output 14 of the controller 1.

[33] A different separator 107, arranged at the output of the counter 100, isolates the most significant bit (MSB) of the count number for the time interval in progress. This bit is then sent to a command input of the multiplexer 105, which instantaneously reproduces the signal received on its first or its second input respectively, at the output 14 when the command input bit is equal to 0 or 1. The signal produced at the output 14 for each time interval is the access address ADDR1 to the memory 10 (RAM1).

[34] The address ADDR1 thus obtained, coded over N-1 bits, is equal to the first partial count number during the time intervals respectively numbered from 0 to 2^N-1, and equal to 2^{N-1}-2 from which the first partial count number is subtracted during the time intervals respectively numbered from 2^N to 2^{N+1}-1.

[35] A second circuit branch within the controller 1, also connected to the output of the counter 100, supplies the access address ADDR2 to the memory 20 (RAM2) for each time interval. In this second branch, a second partial count number for the time interval in progress, over N-1 bits, is obtained by adding 1, with a constant number of bits,

to the count number issued by the counter 100, then subtracting the most significant bit (MSB) and the least significant bit (LSB). When 1 is added, over N+1 bits, the result reverts to the value 0 when the value 2^{N+1} is reached. The second partial count number is obtained by the operator 102 shown in FIGURE 2.

[36] The second partial count number is then sent directly to a first input of a multiplexer 106 inside the controller 1. A digital operator 104, operating on N-1 bits, subtracts the second partial count number from the number $2^{N-1}-1$ and sends the result to a second input of the multiplexer 106.

[37] The output of the multiplexer 106 forms the output 15 of the controller 1.

[38] At the output of the operator 102, the most significant bit (MSB) of the second partial count number is further sent to a command input of the multiplexer 106, which instantaneously reproduces the signal received on its first or its second input respectively, at the output 15 when the command input bit is equal to 0 or 1. The signal produced at the output 15 for each time interval is the access address ADDR2 to the memory 20 (RAM2).

[39] The address ADDR2 thus obtained, coded over N-1 bits, is equal to the second partial count number during the time intervals respectively numbered from 0 to 2^N-2, or numbered 2^{N+1}-1, and equal to 2^{N-1}-1 from which the second partial count number is subtracted during the time intervals respectively numbered from 2^N-1 to 2^{N+1}-2, or numbered 2^N-1.

[40] A separator 109, connected to the output of the separator 107, and connected via its output to the outputs 16 and 13 of the controller 1, isolates the least significant bit (LSB) of the count number for the time interval in progress. The bit issued by the separator 109 then forms the switching signal SW1 issued by the output 16 of the controller 1, and the access command R/W2 issued by the output 13. An inverter 110 connected between the output of the operator 109 and the output 12 of the controller 1 produces the access command R/W1. In this way, for each time interval, the access command R/W1, coded over 1 bit, is the opposite of the least significant bit of the count number for the time interval in progress.

[41] Finally, a logical "AND" operator 111, connected to the output of the separator 107, receives at its input the count number for the time interval in progress, reduced to the N least significant bits, and compares it to 2^N-1. The

output of the logical operator 111 is connected to the output 17 of the controller 1, supplying the switching signal SW2.

[42] Table 1 below gives the values of the first and second partial count numbers, together with the values of the outputs 12 to 17 of the controller 1 disclosed above, for each time interval. For this table, by way of example, N is taken as equal to 3. A sequence of time intervals then includes 8 successive time intervals, numbered from 0 to 7 for the first sequence by the counter 100, and from 8 to 15 for the second sequence.

Time interval counter (100)	First Partial Number (101)	W/R1 (12)	ADDR1 (14)	SW1 (16)	Second partial number (102)	W/R2 (13)	ADDR2 (15)	SW2 (17)
0	00	1	0	0	00	0	0	0
1	00	0	0	1	01	1	1	0
2	01	1	1	0	01	0	1	0
3	01	0	1	1	10	1	2	0
4	10	1	2	0	10	0	2	0
5	10	0	2	1	11	1	3	0
6	11	1	3	0	11	0	3	0
7	11	0	3	1	00	1	3	1
8	00	1	2	0	00	0	3	0
9	00	0	2	1	01	1	2	0
10	01	1	1	0	01	0	2	0
11	01	0	1	1	10	1	1	0
12	10	1	0	0	10	0	1	0
13	10	0	0	1	11	1	0	0
14	11	1	3	0	11	0	0	0
15	11	0	3	1	00	1	0	1
16=0	00	1	0	0	00	0	0	0

Table 1

[43] In Table 1, the first and second partial count numbers are shown as binary numbers.

[44] As shown in the last row of Table 1, identical to the row corresponding to the number 0 time interval, all the values of the time interval counters and outputs 12-17 are repeated cyclically, all being obtained from the cyclic

count number, with a period of 2^{N+1}, issued by the counter 100.

[45] It will be obvious to the person skilled in the art that the same table of values may be obtained with a controller 1 having an internal structure other than that disclosed earlier. It should therefore be understood that the functional diagram in FIGURE 2 represents only one example of controller 1 for implementing the invention, and that any other type of controller issuing identical output signals should be regarded as equivalent.

[46] Each of the two memories 10, 20 is designed for a write or read access mode respectively when the corresponding access command R/W1 or R/W2 is equal to 0 or 1.

[47] The first multiplexer 30 is designed to instantaneously reproduce at its output the signal applied to its first or second input respectively, when the switching signal SW1 applied to the command input of the multiplexer 30 is equal to 0 or 1. In other words, during each time interval, the output signal of the multiplexer 30 is equal to the signal applied to one of its two inputs. The multiplexer 40 has an identical operation to that of

the multiplexer 30, transposed according to the switching signal SW2.

[48] Under these conditions, for N again equal to 3, the operation of the storage device is characterized by Table 2 below, deduced from Table 1:

Time interval counter (100)	Source output (1000, E)	RAM1 access (12)	RAM1 output (31)	RAM2 access (13)	RAM2 output (32)	MUX1 output (42)	MUX2 output (51)	Flip-flop D output (52,S)
0	#0	read	-	write	-/#14	-#14	-/#14	-/#15
1	#1	write	-/#13	read	-	-/#13	-/#13	-/#14
2	#2	read	-	write	-/#12	-/#12	-/#12	-/#13
3	#3	write	-/#11	read	-	-/#11	-/#11	-/#12
4	#4	read	-	write	-/#10	-/#10	-/#10	-/#11
5	#5	write	-/#9	read	-	-/#9	-/#9	-/#10
6	#6	read	-	write	-/#8	-/#8	-/#8	-/#9
7	#7	write	-/#15	read	-	-/#15	-/#7	-/#8
8	#8	read	-	write	#6	#6	#6	#7
9	#9	write	#5	read	-	#5	#5	#6
10	#10	read	-	write	#4	#4	#4	#5
11	#11	write	#3	read	-	#3	#3	#4
12	#12	read	-	write	#2	#2	#2	#3
13	#13	write	#1	read	-	#1	#1	#2
14	#14	read	-	write	#0	#0	#0	#1
15	#15	write	#7	read	-	#7	#15	#0

Table 2

[49] In Table 2, each # sign indicates an identification number for the datum concerned, identified with respect to the time interval during which the source 1000 has produced this datum (second column of Table 2). When two alternative references are entered in a box of Table 2, the first reference corresponds to the value taken during a first execution of the storage device operating cycle, and the second reference corresponds to the value taken when the device's operating cycle has already been previously executed. A dash shown instead of a reference means the absence of any determined value for the output concerned, which occurs at the time of a first execution of the cycle, or corresponds to an operation not ending up in the issue of a determined value.

[50] By comparing the last column of Table 2 showing the data successively issued by the output S of the device with the data produced at the input E (second column of Table 2), it can be seen that the operation of the storage device actually corresponds to that of a reverse stack of depth $2^N=2^3=8$.

[51] It will be apparent to the person skilled in the art that the address ADDR1 and access command R/W1 values shown in Table 1 for the time intervals 2^N-2, 2^N-1, $2^{N+1}-2$ and

2^{N+1}-1 can be replaced by other values, under condition that these replacements have no effect on the contents of the memory 10 written during the other time intervals. The overall reverse stack operation of Table 2 (last column of Table 2) then remains unchanged. Similarly, the values of ADDR2 and R/W2 shown for the time intervals 2^{N}-1 and 2^{N+1}-1 can be modified under the same conditions.

[52] A second embodiment of a storage device according to the invention is now disclosed, which uses two immediate read SP-RAM type memory modules. The architecture of the device shown in FIGURE 1 is used again for this second embodiment.

[53] FIGURE 3 shows the functional diagram of a controller 100 adapted for using immediate read SP-RAM memories. The controller 1 again includes counters 100, 101 and 102 based on the time interval in progress, identical to those disclosed in the first embodiment. The outputs of the counters 101 and 102 are respectively connected to the first inputs of the multiplexers 105 and 106. Furthermore, the outputs of the counters 101 and 102 are also connected to the inputs of two identical digital operators 103' and 104', each operating over N-1 bits. The operators 103' and 104' each subtract the values received as input from 2^{N-1}-1.

The output of the operator 103' is connected to the second input of the multiplexer 106, and that of the operator 104' is connected to the second input of the multiplexer 105.

[54] Both multiplexers 105 and 106 receive at their respective command input, the most significant bit (MSB) of the count number for the time interval in progress produced by the counter 100. This most significant bit (MSB) is isolated by the separator 107. The multiplexers 105, 106 are set up to instantaneously reproduce at their respective output the signal received at their respective first or second input, when the signal received at their command input is equal to 0 or 1, respectively.

[55] The output of the multiplexer 105 is connected to the output 14 of the controller 1, transmitting the address ADDR1, and the output of the multiplexer 106 is connected to the output 15, transmitting the address ADDR2.

[56] The separator 107 further issues the N least significant bits (LSB) of the count number for the time interval in progress to the logical "AND" operator 111. The operator 111 compares the value received at its input with 2^N-1, and issues at its output the binary signal 1 in the event of equality, otherwise the binary signal 0. This binary signal is sent to an inverter 112, whose output

generates the second switching signal SW2 and is connected to the output 17 of the controller 1.

[57] The separator 108 isolates the least significant bit (LSB) of the count number for the time interval in progress, and is connected to the input of the inverter 113. The outputs of the separator 107 and the inverter 113 respectively issuing the most significant bit (MSB) and a binary signal opposite to the least significant bit (LSB) of the count number for the time interval in progress are connected to the inputs of the logical operator 114, performing the "exclusive OR" logical operation, marked "EXCL_OR". A logical "OR" operator 115 receives as inputs the binary signals produced by the operators 111 and 114, and produces as output the access command R/W1 transmitted onto the output 12 of the controller 1. Finally, an inverter 116 produces the access command R/W2 from the output signal of the operator 115, and is connected to the output 13 of the controller 1. The signal SW1 transmitted onto the output 16 is identical to the access command R/W2.

[58] Thus, the access commands R/W1 and R/W2 correspond, for each time interval, to the respective expressions:

$$R/W1=[^{C}C(0))\ \text{EXCL\_OR}\ C(N))]\ \text{OR}\ ^{C}[SW2],\ \text{and}$$

$$R/W2=[C(0)\ \text{EXCL\_OR}\ C(N)]\ \text{OR}\ ^{C}[SW2],\ \text{where:}$$

C(0) is the least significant bit (LSB) of the time interval in progress,

C(N) is the most significant bit (MSB) of the time interval in progress,

^{C}X designates the opposite value to the binary value X.

[59] We can also use: $R/W2=^{C}R/W1$, R/W1 being again given by the first of the two formulae above.

[60] The "OR" operator 115 may possibly be eliminated, together with its connection to the input of the operator 112. The output of the "EXCL_OR" operator 114 is then directly connected to the outputs 12 and 16 of the controller 1 and to the input of the inverter 116. The previous formulae then become:

$$R/W1=[^{C}C(0))\ \text{EXCL\_OR}\ C(N))], \text{ and}$$

$$R/W2=^{C}R/W1.$$

[61] Table 1a below corresponds to Table 1, transposed to the second embodiment, N again being taken as equal to 3, by way of example:

Time interval counter (100)	First partial number (101)	W/R1 (12)	ADDR1 (14)	SW1 (16)	Second partial number (102)	W/R2 (13)	ADDR2 (15)	SW2 (17)
0	00	1	0	0	00	0	0	1
1	00	0	0	1	01	1	1	1
2	01	1	1	0	01	0	1	1
3	01	0	1	1	10	1	2	1
4	10	1	2	0	10	0	2	1
5	10	0	2	1	11	1	3	1
6	11	1	3	0	11	0	3	1
7	11	0	3	1	00	1	0	0
8	00	0	3	1	00	1	3	1
9	00	1	2	0	01	0	3	1
10	01	0	2	1	01	1	2	1
11	01	1	1	0	10	0	2	1
12	10	0	1	1	10	1	1	1
13	10	1	0	0	11	0	1	1
14	11	0	0	1	11	1	0	1
15	11	1	3	0	00	0	0	0
16=0	00	1	0	0	00	0	0	1

Table 1a

[62] The memories 10 and 20 and the multiplexers 30 and 40 each have identical operations to those disclosed for the first embodiment. Table 2a below is then deduced from Table 1a in reference to FIGURE 1:

Time interval counter (100)	Source output (1000,E)	RAM1 access (12)	RAM1 output (31)	RAM2 access (13)	RAM2 output (32)	MUX1 output (42)	MUX2 output (51)	Poret D output (52, S)
0	#0	read	-/#14	write	-	-/#14	-/#14	-/#15
1	#1	write	-	read	-/#13	-/#13	-/#13	-/#14
2	#2	read	-/#12	write	-	-#12	-#12	-/#13
3	#3	write	-	read	-/#11	-/#11	-#11	-/#12
4	#4	read	-/#10	write	-	-/#10	-/#10	-/#11
5	#5	write	-	read	-/#9	-/#9	-/#9	-/#10
6	#6	read	-/#8	write	-	-/#8	-/#8	-/#9
7	#7	write	-	read	-/#0	-/#0	-/#7	-/#8
8	#8	write	-	read	#6	#6	#6	#7
9	#9	read	#5	write	-	#5	#5	#6
10	#10	write	-	read	#4	#4	#4	#5
11	#11	read	#3	write	-	#3	#3	#4
12	#12	write	-	read	#2	#2	#2	#3
13	#13	read	#1	write	-	#1	#1	#2
14	#14	write	-	read	#0	#0	#0	#1
15	#15	write	-	read	#0	#0	#15	#0

Table 2a

[63] It will be obvious to the person skilled in the art on looking at Tables 1a and 2a that the access command and address values R/W1, ADDR1, R/W2 and ADDR2 can be replaced by values without any effect on the contents of the memories 10, 20 for instants 2^N-1 and 2^{N+1}-1. The data

issued at each time interval by the storage device then remain identical.

[64] The second embodiment again matches well with an operation of a reverse stack of depth 2^N.

[65] It is understood that, for both embodiments disclosed, the memories 10, 20 and the multiplexers 30, 40, 105 and 106 may be replaced by similar elements for which the access commands or the switching signals are the reverse of those mentioned earlier. Accordingly, the controller 1 must then be adapted, without the principle of the invention and the architecture of the storage device depicted in FIGURE 1 being modified.

[66] Although preferred embodiments of the method and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.